

Possibilities and Limits of an automated AE-Channel-Verification Process

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1. Abstract

The European standard CEN EN 13477-2 defines how the verification of the AE-channel for AE-burst measurement has to be performed. The manually controlled generation of the many different test signals required and reporting the results is rather a time consuming matter and calls for a combined hardware/software tool for the automation of this process.

This paper describes a possible and realized solution for an automated AE-channel verification that has been designed for Vallen equipment, but is here expressly made public, for royalty free adaptation to other manufactures of burst-AE-systems.

The verification process here described is for several months in use for post-configuration / pre-despatch verification at the Vallen factory, but can also be made available to each user of Vallen AE-channels of model ASIPP. It requires

- an arbitrary waveform generator (Agilent 33120A/33220A),
- software for the test signal stimulation (Vallen VeriStimulator) and a special printer cable to the “Externals” connector of AMSY4 or AMSY-5
- the normal AE-burst data acquisition program of the AE-system (Acqui32), and
- software for the verification of the measurements and for report generation (Vallen VeriAnalyzer).

The paper also discusses some problems and potential improvements of EN13477-2.

2. Introduction

The scope of EN13477-2 says “This .. standard specifies methods for routine verification of the performance of an AE equipment comprising one or more sensing channels. It is intended for use by operators of the equipment. Verification of the measurement characteristics is recommended after purchase of equipment, modifications or use under extraordinary conditions.” The need of routine verification is mentioned in the first sentence.

The procedures described in EN13477-2 do not exclude other qualified methods. The automated verification method can use a larger variety of test signals than required by EN13477-2, and leads to a report that represents much more information about the accuracy of the measurements the AE channel performs.

EN13477-2 describes methods for the verification of sensor sensitivity and noise, preamplifier performance and the signal conditioning and measurement system.

This paper concentrates on the most expensive, because most time consuming part of this verification, the verification of the AE-signal processor (ASIPP). Since thousands of those AE

signal processors are in use world wide, and have to be verified in a routinely manner, the total costs spent on AE channel verification can be dramatically reduced by an automated verification process.

3. Hardware requirements

Fig. 1 shows the hardware setup of the automated AE-channel verification. The PC controls the AE-system over a high-speed PCI-interface board (ASyC). For the verification, the PC also controls an arbitrary function generator of model 33120A (over RS232) or 33220A (USB/Ethernet) and over a parallel cable the data recording and a parametric counter inputs in the AE system.

The stimulation control software controls over LPT1 parallel interface data recording and the parametric counter (PCTD) of the AE system. PCTD is used as a pointer into a table of test signal parameters. This table tells the analysis program for each PCTD value the corresponding “should be” values for the measured AE parameters.

The only “special” hardware, beside of the function generator, is the cable from LPT1 connector of the PC to the “Externals” connector of the AMSY-5. The schematic for that cable is shown in the corresponding documentation.

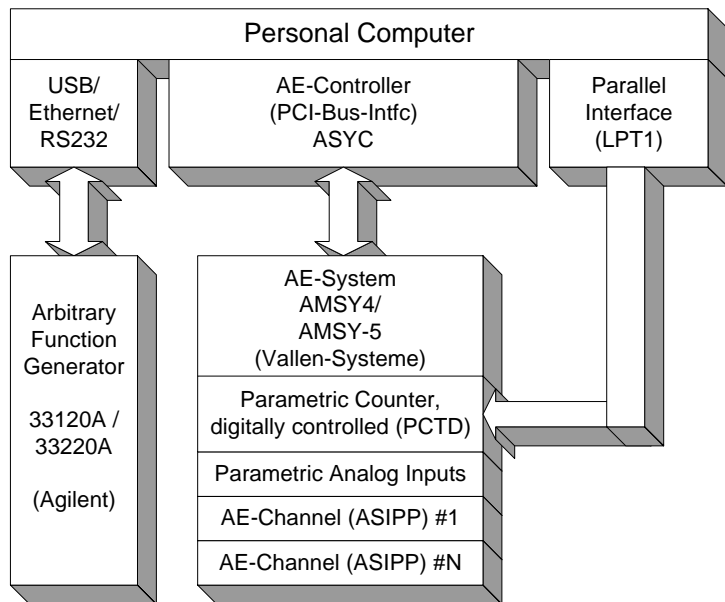


Fig. 1: Hardware requirements for automated verification

4. Channel verification software

The automated verification process runs in two phases, a signal stimulation and data acquisition phase, followed by the data verification phase. Accordingly, the following software components are used:

“**VeriStimulator**” programs a number of test patterns into the function generator and controls the generation of test patterns in a certain sequence. For the AE-Channel verification there are three semi-automatic steps:

In Step 1, there are several variations of parameters (duration, amplitude at a certain working frequency in the middle of the bandwidth of the channel, plus a frequency response test.)

Step 2 is optional and determines the frequency response of the optional 2nd filter module.

Step 3 is to verify the proper working of the auto-calibration feature.

The delay items offered in the menu (Fig. 2) are to adapt the software to older versions of Vallen AE-Systems.

During the course of the signal stimulation phase, VeriStimulator directs the user to make changes in the connections, when needed.

This happens for example, when a channel is complete and the cable from the function generator shall be connected to the next channel.

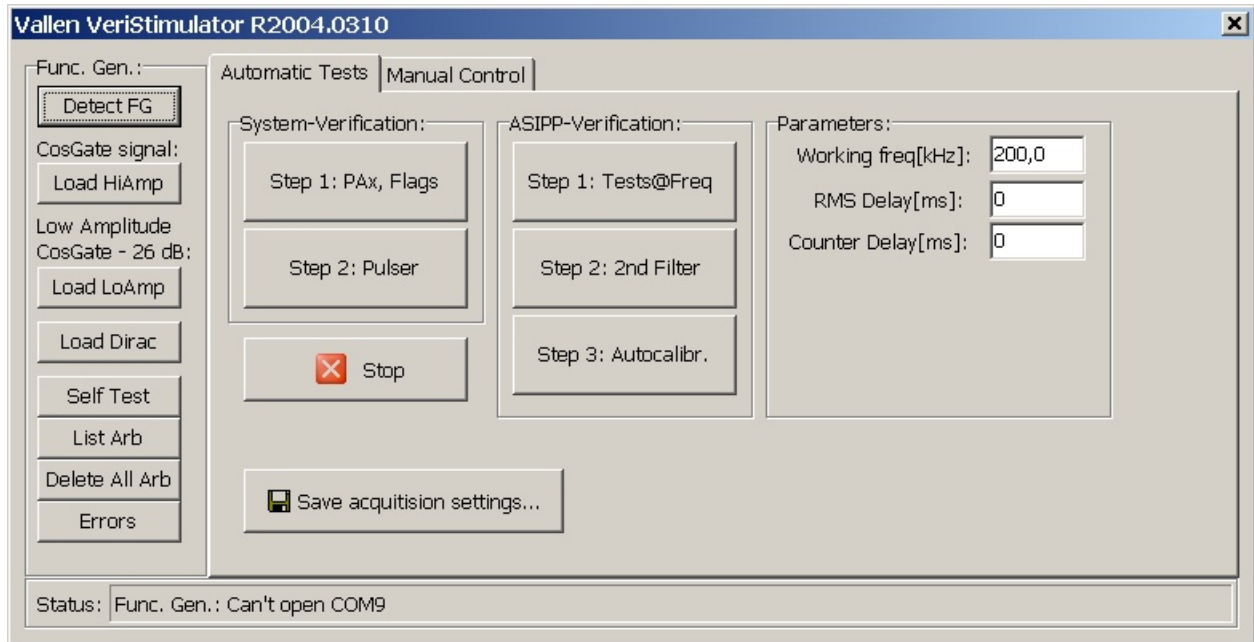


Fig. 2: VeriStimulator Setup

“**Acquisition32**” is the normal data acquisition program used to acquire AE data and store them onto the hard disk of the PC. This program doesn’t “know” whether it is used for normal data acquisition or for the automated verification process. It acts as usual. The identification of the verification patterns is stored in the parametric data that attend the AE burst data as usual.

“**VeriAnalyzer**” is an offline program that reads AE data from file, identifies whether (or not) the data were stimulated by a valid release of “VeriStimulator” and analyses the “Should Be” values for each stimulated burst, and creates a report in Word format. This report contains a number of Diagrams that are described below.

5. Testsignals and result examples

The automated verification process uses the following kinds of test signals which are stimulated by the arbitrary function generator under software control:

5.1 Single Dirac Pulses:

This is a sharp pulse (Fig. 3) . Used to trigger a hit for passing administrative information (in the parametric counter PCTD) to the VeriAnalyzer software:

- To indicate the data format (version id) of VeriStimulator,
- To open or close a certain test series (e.g. the variation of a certain AE parameter).

See set 633 in Fig. 6. PCTD=18 initiates a series of duration varied hits. PCTD=2 closes the series, PCTD=70 to 86 point into a “should be” table of durations for this verification step.

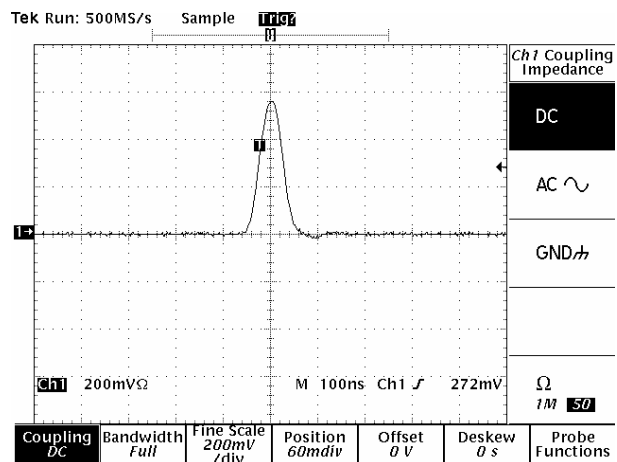


Fig. 3 Dirac Pulse, 50ns width (at 50% amp.)

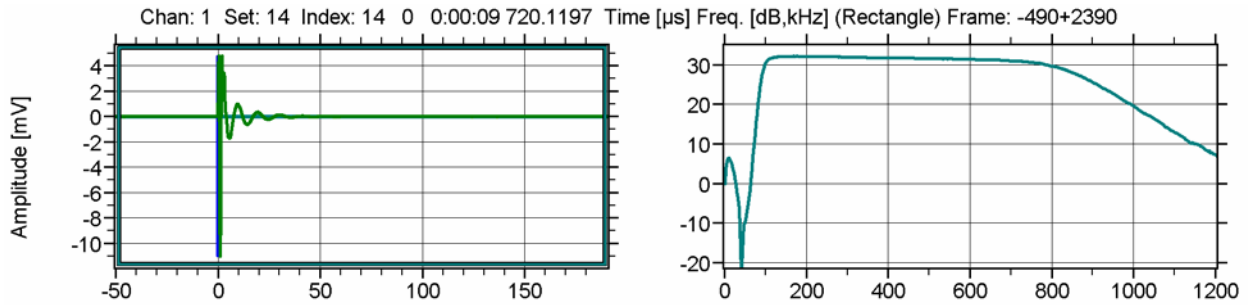


Fig. 4: ASIPP response (95-850kHz) to Dirac Pulse Input. Left in time domain, right the FFT

5.2 Rectangular-shaped burst:

Used to vary Duration and to check the parameters Duration, Energy, Counts.

Problems: Settling behaviour with overshoot at the beginning, and the ring-down behaviour at the end (see Fig. 5) influence the AE parameters Peak Amplitude, Risetime, Duration, Enery, Counts. Needs some intelligent correction.

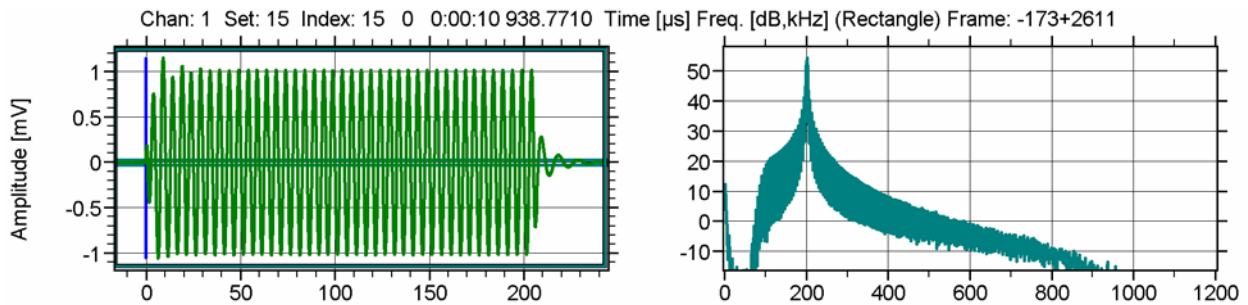


Fig. 5: ASIPP Response on a rectangular shaped sine wave burst .

5.3 Listing example for the duration variation test

Id	DSET	CHAN	PCTD	A	R	D	E	CNTS	Comment:
				[dB]	[μs]	[μs]	[eu]		
Ht	633	1	18	81,0	1,2	42,8	885E01	5	Dirac: Open
Ht	744	1	70	61,4	9,0	225,4	106E02	43	Testptrn #1
Ht	817	1	72	61,4	9,0	449,6	219E02	88	Testptrn #2
Ht	891	1	74	61,4	9,0	919,6	462E02	182	Testptrn #3
Ht	971	1	76	61,4	9,0	1919,2	979E02	382	Testptrn #4
Ht	1053	1	78	61,4	9,0	4024,0	207E03	802	Testptrn #5
Ht	1126	1	80	61,4	9,0	8483,2	437E03	1695	Testptrn #6
Ht	1199	1	82	61,4	9,0	17907,2	925E03	3580	Testptrn #7
Ht	1290	1	84	61,1	9,0	37836,8	195E04	7568	Testptrn #8
Ht	1362	1	86	61,4	9,0	80000,0	413E04	16000	Testptrn #9
Ht	1492	1	2	75,0	1,2	36,4	220E01	4	Dirac: Close

Fig. 6: Listing of a test with duration variations (initiated by PCTD=18 and closed by PCTD=2) see signal 3.1 above. PCTD = parametric counter digitally controlled. Each PCTD value identifies a test signal and the corresponding "should be" results

5.4 Deviation diagram example for the duration variation test (Test #3)

The verification report shows a number of "Deviation Diagrams", which contain graphical and numerical results. The horizontal position of each dot in a diagram represents a "should be" value, and the vertical position represents the deviation of the measured value from that "should be" value, in percent or dB as given in the legend. The meaning of each diagram (axis results) and some additional numerical values are shown in different parts of the legend.

Test 3: Duration variation:

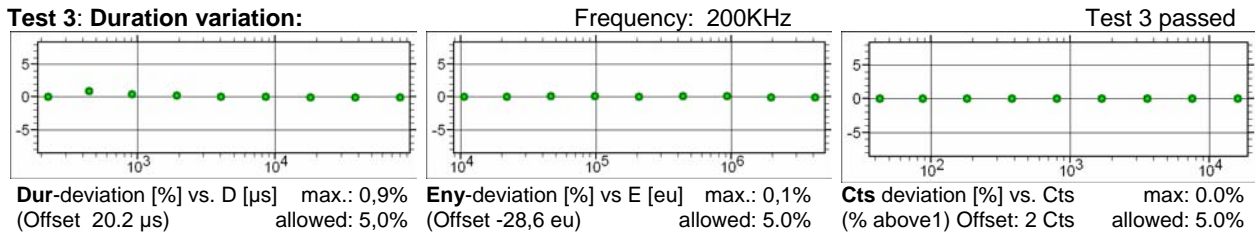


Fig. 7: Results in Fig. 6 shown in three "deviation" diagrams.

The "Offsets" indicated in the legends of Fig. 7 were determined by the deviation of the first (shortest) measured signal from the "should be" values and applied to all 9 signals to correct the influence of the settling behavior and ring down effects.

5.5 Dirac Series:

Such series are used to check duration discrimination and rearm timing (internal time parameters).

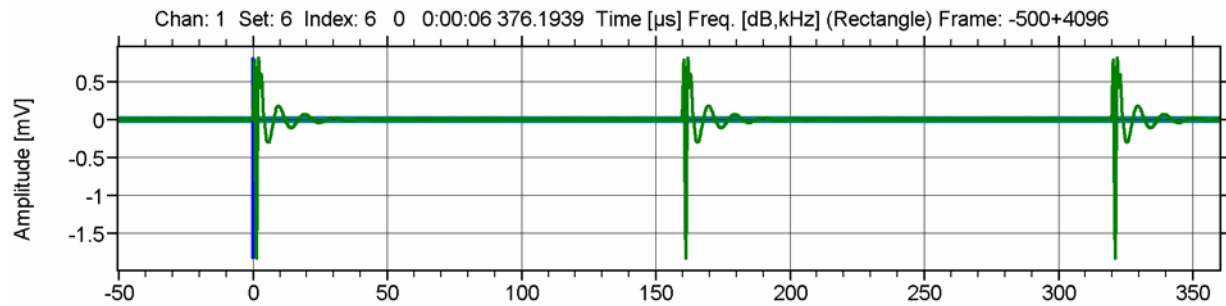


Fig. 8: Response to a series of Dirac Pulses

5.6 Sine-square-shaped burst:

This is a sine wave burst in an envelope of a sine-square shape (Fig. 9).

This burst consist of 48 samples/sinewave and 41 sinewaves for the burst, this gives a sequence of 1968 samples for the complete test signal. These "sine-square-shaped test signals are used with (sampling) frequency variation at fixed amplitude to measure

- Frequency response (no need for transient recorder),
- Rise-time response; and with amplitude variation at fixed frequency to measure
- Peak amplitude response (linearity)
- Energy response (squared or non-squared).

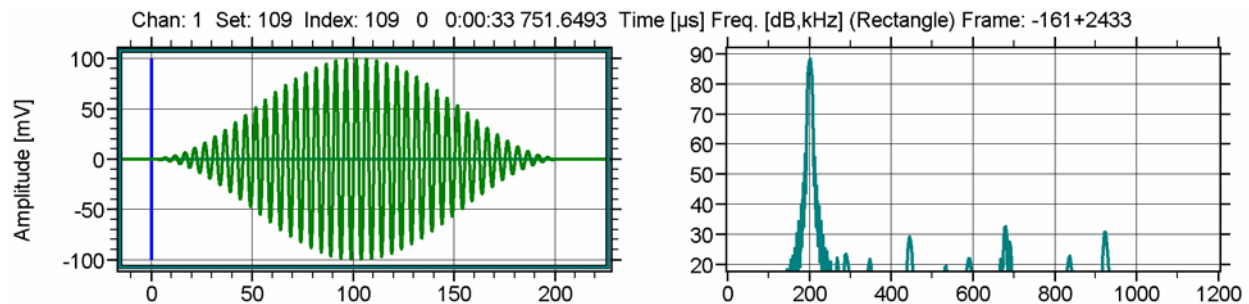


Fig. 9: Response to a sine-square-shaped burst.

The impurities in the FFT (above 220kHz, right diagram) are produced by the test generator..

5.7 Data example: Frequency and rise time response

Fig. 10 shows results of test #4, where test signals of different frequencies (sine-square-shaped) were used. The upper diagram shows dB_{AE} values over the frequency. Above the diagram the software places the found 3db bandwidth limits. The lower diagram shows the rise time-deviation vs rise time (the should be values) of those signals that were measured with an amplitude above maximum – 1dB.

Since the rise time is defined as the time from first threshold crossing to peak amplitude detection, and the sine-square shaped test signal begins very smoothly, noise may contribute to some uncertainty of the exact time of the 1st threshold crossing.

As can be seen in Fig. 9, the peak time is also difficult to determine. Due to these inherent uncertainties, a deviation of 10% for the rise time is shown as the allowed tolerance.

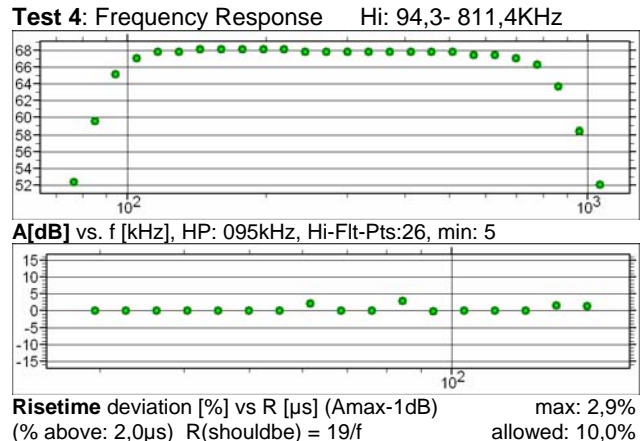


Fig. 10 Results of frequency variation: Frequency response and rise time deviation

5.8 Data example: Amplitude variation, amplitude and energy response

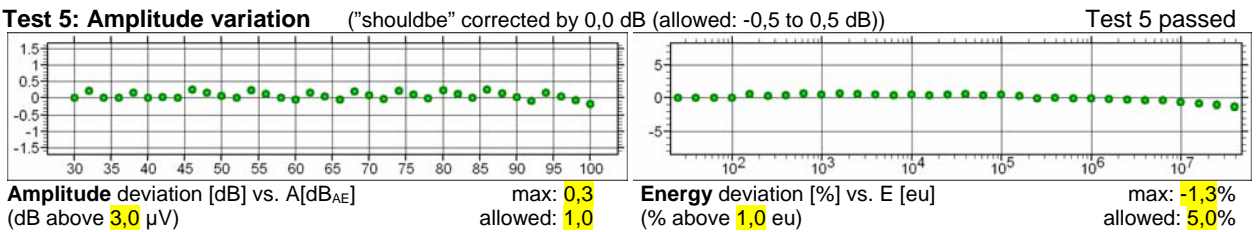


Fig.11: Example for amplitude and energy deviation diagrams (Test #5 of verification). A correction of the "should be" values for balanced positive and negative deviations is shown above the diagram.

These amplitude variation results are obtained using sine-square-shaped signals, because these do not show the settling behaviour we see with rectangle shaped signals. Here, one difficulty was the limited dynamic range of the function generator, that is only programmable in a 46dB range, but we need to check a dynamic range of 70dB (30..100dB_{AE}). The increase of dynamic range for the function generator was solved by using a second sine-squared shape in a lower amplitude range.

No external attenuator is needed and the full dynamic range can be tested without a change of the threshold setting.

Another difficulty can be shown in the listing of the amplitude-varied signals below. Usually, PCTD is incremented by 2 between two test signals. Below there are two occurrences where PCTD stayed constant (140, 150). Two unexpected signals of low amplitude (about 30dB) were triggered by noise from the function generator. However, those noise signals can be identified by the verification analyzer software and do not disturb the verification result as long as the signal with expected amplitude for each PCTD value can be found in the data.

Data Example:

Id	DSET	CHAN	PCTD	A	R	D	E	CNTS
				[dB]	[μ s]	[μ s]	[eu]	
Ht	3912	1	138	78,0	97,6	196,2	248E03	39
Ht	3931	1	140	30,6	0,2	15,0	882E-3	1 ←A=30,6dB
Ht	3933	1	140	80,2	97,8	196,4	392E03	39
Ht	3969	1	142	82,1	97,8	198,6	622E03	40
Ht	3989	1	144	84,0	97,8	198,8	986E03	40
Ht	4009	1	146	86,3	99,4	200,8	156E04	40
Ht	4029	1	148	88,1	99,8	201,2	247E04	40
Ht	4048	1	150	31,3	0,2	57,4	592E-3	1 ←A=31,3dB
Ht	4067	1	150	90,0	99,8	201,4	391E04	40
Ht	4087	1	152	91,9	100,0	201,8	620E04	40
Ht	4108	1	154	94,2	100,0	202,2	980E04	40
Ht	4146	1	156	96,0	101,4	205,4	155E05	41
Ht	4165	1	158	97,9	101,6	210,8	245E05	42
Ht	4202	1	160	99,8	104,2	212,8	387E05	42

Fig. 12: Listing of Test #5:

Amplitude variation in 2dB steps (Extract).

Problem: False hits (A < 32dB) triggered by noise of function generator.

Such noise is eliminated by VeriAnalyzer, because only the last hit of PCTD-ID counts.

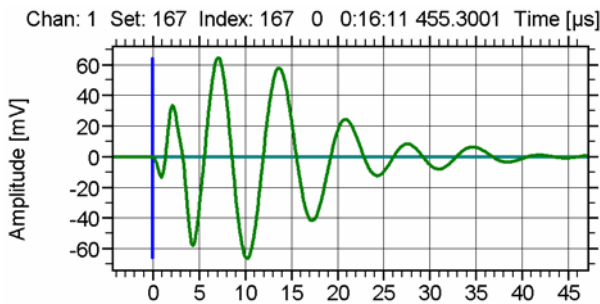


Fig. 13: Calibration Pulse Response

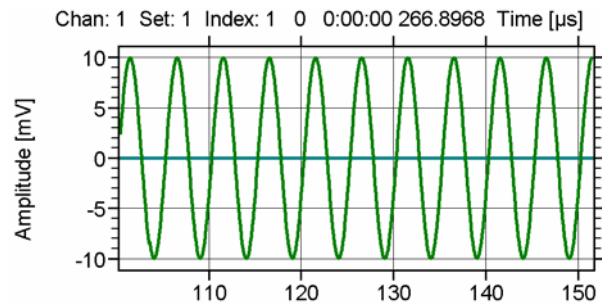


Fig. 14: Continuous sine wave

5.9 Calibration Pulse Response:

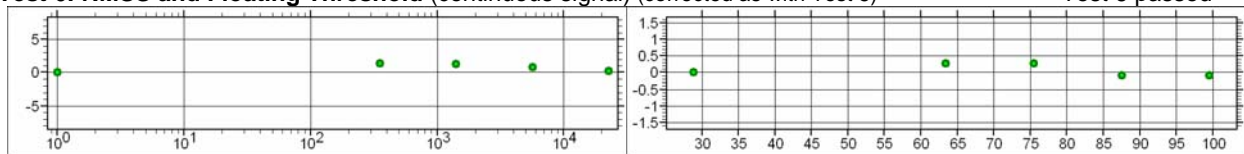
This test signal (Fig. 13 shows the response) is only used to check whether the calibration pass works. There is no accuracy check required, because the pulse signal is checked during the system verification run (performed by the same program but not described in detail here)

5.10 Continuous sine wave:

This test signal (Fig. 14) is used to verify the accuracy of background noise measurement and the floating threshold behaviour. Due to the limited dynamic range of the function generator, 300 μ V_{RMS} is the lowest level that can be verified.

Test 6: RMSS and Floating Threshold (continuous signal) (corrected as with Test 5)

Test 6 passed



RMSS deviation [%] vs. RMSS [μ V]
(% above 2,0 μ V)

max: 1,4%
allowed: 5,0%

Floating Threshold deviation [dB] vs THR[dBAE] max: 0,3
(dB above 1,0 μ V) TNR:4,2 allowed: 1,0

Fig. 15: Result of verification of background noise and floating threshold behaviour (Test #6)



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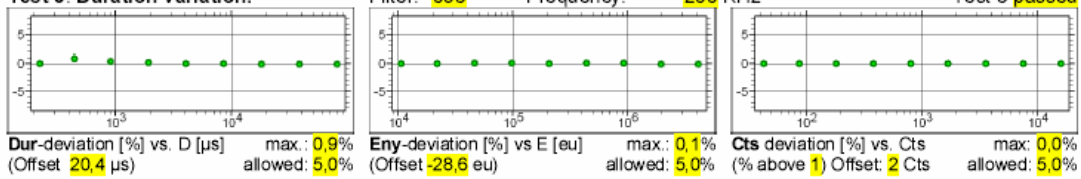
The Acoustic Emission Company

AMSY-5 ASIPP Verification Report

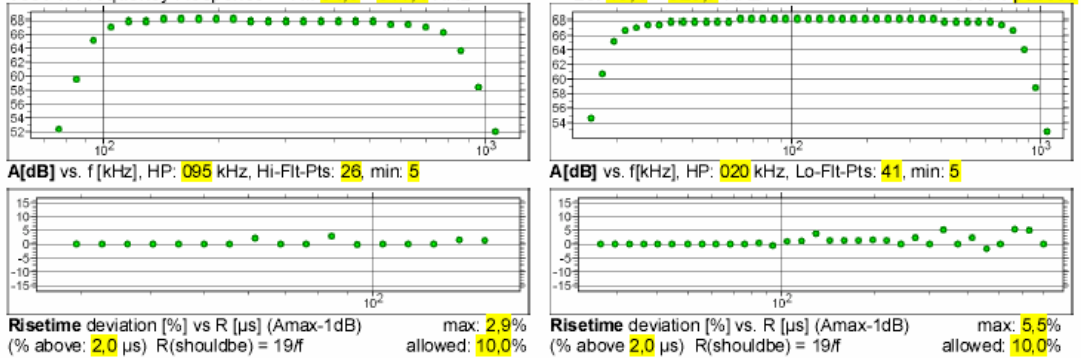
VeriAnalyzer Rev. 2004.0310 Data Format: 00.01 ASIPP.Template.doc-Rev.: 23/05/2004 12:33

Channel: 1 (HW: 01.01) ASIPP No.: 2060 Rev HW: 4.2 FW: R3 Box IdNo: 42683
 Filter 1-Hi: 095 Filter 2-Lo: 020 TP4: 850 ASP-SQY: Y TR-4M: Y Energy: true
 Signal Source: Agilent 33x20A IdNo: 42294 calibrated till: 04/05. Signal fed-in at BNC connector "AC"

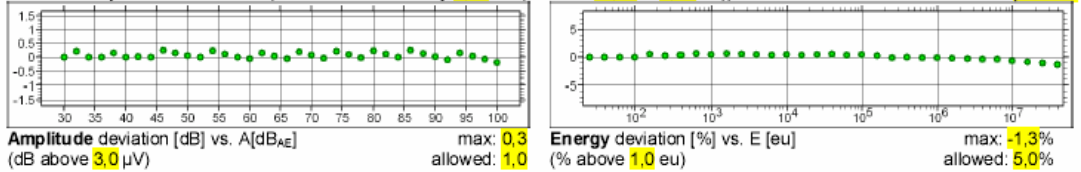
Test 1: Cascaded hits 80µs apart. Hits: 1 (1) Cascaded Hits: 3 (3) Test 1 passed
 Test 2: 12 hits 125µs apart: Hits: 12 (12) Cascaded Hits: 12 (12) Test 2 passed
 Test 3: Duration variation: Filter: 095 Frequency: 200 KHz Test 3 passed



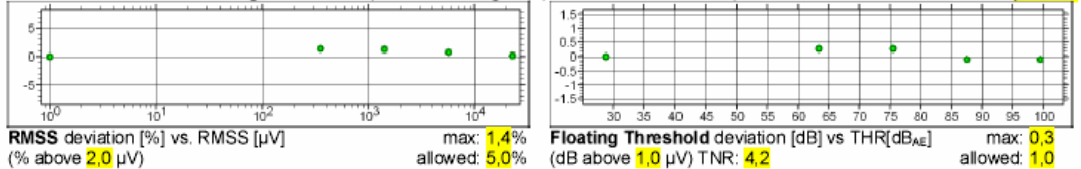
Test 4: Frequency Response Hi: 94,3 - 811,4 KHz Lo: 19,4 - 823,7 KHz Test 4 passed



Test 5: Amplitude variation (shouldbe corrected by 0,00 dB (allowed: -0,50 to 0,50 dB)) Test 5 passed



Test 6: RMSS and Floating Threshold (continuous signal) (corrected as with Test 5) Test 6 passed



Test 7: Autocalibration pulser path: Test 7 passed
 Pulser Voltage: 200,0 V, Calib.Amp. (no cable connected, filter 1 - Hi): 90,0 dB, should be: (>55dB)

All tests passed Icking, 23.05.2004 12:30, verified by [User: hv] (initials): _____ Sign: _____

Fig. 16: Example of an automatically generated AE channel verification report. The yellow fields are place holders and filled with text by the report generator.

6. Software sub-components contributing to the report generation

6.1 VeriConfig.doc is a Word (*.doc) file filled-in by the operator. This report identifies all relevant configuration information for the verification process, among them

- the type, ID number and current address of the AE-system in which the AE-channels are installed for verification,
- the identification and recalibration dates of the used test signal generators, and for each AE channel:
- the ID number and current address of each AE-channel,
- the channel’s hardware and firmware revision,
- the installed options (squarer, transient recorder, and bandwidth limits of the frequency filters).

An extract of that report is shown in Fig. 17

AMSY-5 ASIPP Configuration Report												
VeriConfig.Template: 4/28/2004 3:20 PM Version 3.0												
The contents of this document are used for the generation of one verification report per ASIPP by Y5VeriAnal												
System Type	IdNo	Rad Addr	No of PA-Channels	Ref ASIPP Id	Ref ASIPP Ch No							
AMSY-5 M16	42683	01	4	41814	60							
Signal Source used for PAx Input Stimulation: Analogic AN3100 IdNo: 40806 calibrated till: 06/04												
Signal Source used for ASIPP-Verification: Agilent 33x20A IdNo: 42294 calibrated till: 04/05												
ASIPP Chan No.	Prüf No.	Rev.		ASP-SQ (Y/N)	O K	TR-4M (Y/N)	O K	High-Pass 1 (Hi) HP4-	High-Pass 2 (Lo) HP4- / BP-	Low-Pass TP4-	Remark	Verified
		H W	F W									
1	2060	4.2	R3	Y	✓	Y	✓	095	020	850		✓
2	2061	4.2	R3	Y	✓	N		095	020	850		✓
3	2062	4.2	R3	Y	✓	N		095	020	850		✓
4	2063	4.2	R3	Y	✓	N		095	020	850		✓
5	2064	4.2	R3	Y	✓	N		095	020	850		✓

Fig. 17: Extract of VeriConfig.doc filled in with details about the configuration of a system and the devices used for test signal generation.

The hardware configuration of an AE-system is detected, analysed and stored onto the AE data file by the data acquisition program. VeriConfig.doc is read by “VeriAnalyzer” and compared with the hardware configuration found on the AE data file. Configuration mismatches are reported immediately. Some configuration items have influence on the “Should Be” values (e.g. the method of energy determination), some are only used for inclusion into the report. VeriConfig.doc has no influence on VeriStimulator.

6.2 ASIPPTemplate.doc is a Word (*.doc) template file used by “VeriAnalyzer” for report generation. It contains text marks and diagram place holders where VeriAnalyzer inserts results in numerical or graphical presentation. The letter head and company logo are part of the template and shall identify the organization that performs the verification.

Fig. 18 shows an extract of the template used for the report in Fig. 16.

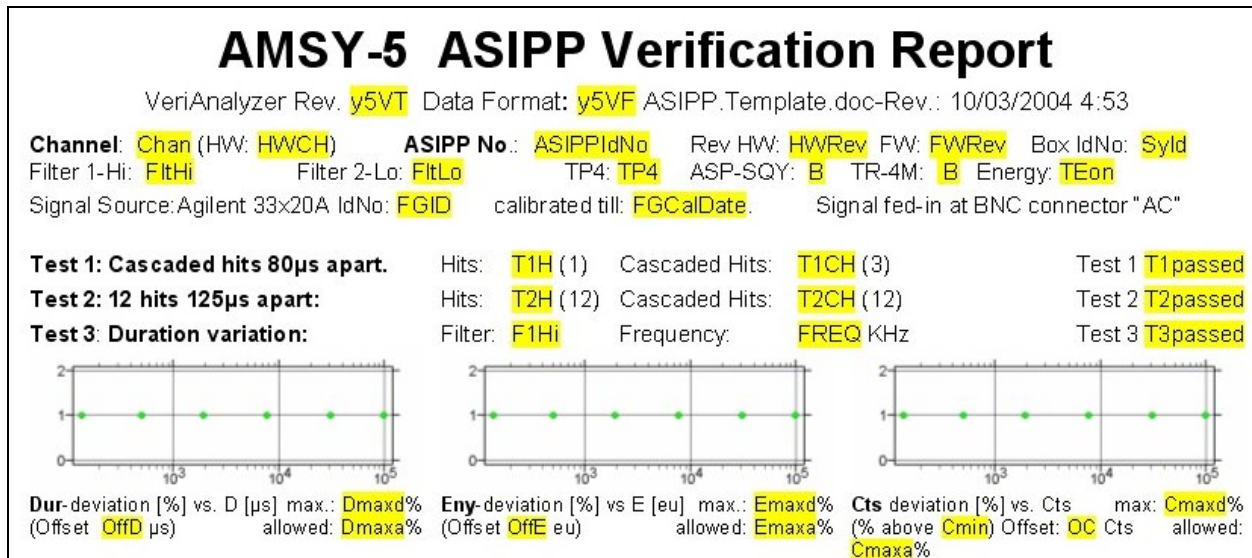


Fig. 18: Extract of ASIPPTemplate.doc. The yellow marked text-fields and the diagrams are just place holders (variables) to be replaced by VeriAnalyzer. See Fig. 16

7. Conclusions

Since the only calibrated equipment needed for the channel verification process is a commercially available function generator from mass production, the costs of keeping that in a calibrated state are low and affordable for almost each owner of an AE system.

The manually performed channel verification is a very time consuming process because of the many settings required for test signal variation.

With automated verification as described above the number of different test signals is not a limiting point. Much more signal variants can be generated, verified and reported.

For the reporting of verification results a combination of “deviation diagrams” and relevant legend information have been developed. A lot of verified measurements can be presented in very dense form that way.

Side effects such as the settling behaviour of rectangle shaped bursts can be minimized by determining the deviation in duration, energy and counts of the shortest burst, and apply the so determined “offsets” to all measurements.

The best suited signal shape of high frequency purity is the sine-square-shaped envelope. The envelope increases and decreases very smoothly. The determination of the rise time, defined as the time period from the first threshold crossing to the highest peak amplitude in the signal, bears some uncertainty, because the first threshold crossing as well as the peak amplitude lies in the time periods of the lowest changes in amplitude.

Not shown in the paper are side benefits. For example, an incremental storage of all verification results of all channels may lead to statistical results about the scattering in parameter results, depending on e.g. the filter configuration or other variables.

The verification process presented could easily be adopted to other manufactures of AE equipment.