A FPGA Based Platform for Multi-Frequency Eddy Current Testing

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Abstract
We developed a highly integrated, Field Programmable Gate Array (FPGA)-based digital multi-frequency eddy current platform which is capable of detecting surface breaking and subsurface cracks in non-magnetic plates. Excitation signal generation, receiving signal demodulation, and USB communication were all implemented inside a Xilinx FPGA (Spartan III). Multi-frequency test results provide rich information about a crack and form the base for crack characterization and identification.

Keywords: materials characterization, in-process, signal processing, eddy current testing (ECT), Electromagnetic Testing (ET), Field Programmable Gate Array (FPGA)

1 Introduction
Non-magnetic metallic materials are used in a wide range of industrial applications, such as the petroleum, chemical, pharmaceutical, and energy industries [1]; as a result, the necessity to assess the natural degradation, such as corrosion, loss metal, surface cracks, subsurface ones, and external factors (third party damage, for instance), requires scientists and engineers to develop new solutions and improve the existing methods to carry out the evaluation of these materials.

In order to perform the evaluation, many different methods can be applied for the task, such as optical, X-ray, and ultrasonic method. Some of these methods can be hazardous, bearing relative high cost or involving complex processes. Eddy current methods [2][3], due to the advantages it offers, namely: low-cost, high speed of evaluation and contactless operation, have attracted the attentions of researchers from industries and research institutes.

Advances in electronics components allow a digital eddy current instrument to be constructed. Multi-frequency excitation signals generation, data acquisition, post processing (demodulation) and the communication with the PC host, are the purpose of the work presented in this paper. Section 2 presents a brief description of the theory behind the instrument; section 3 describes the hardware and software integration and explains the method used to perform the demodulation for single and multi-frequency respectively. The results section describes the evaluation process for the multi-frequency platform and the SNR of the system. The last section covers the conclusion.

2 Background Theory
The inductive principle is the basis of the eddy current instrument used in this paper, which can be explained using the Faraday’s law.

\[
\nabla \times \mathbf{E} = -\frac{\partial \mathbf{B}}{\partial t}
\]
As a consequence of using the induction, the instrument can be contactless, giving an advantage to the method [4]. The instrument consists of two coils, the excitation coil and the receiver coil; the process can be described as follows [5]: a sinusoidal current is applied to an excitation coil, which generates a primary magnetic field; if a conductive object is placed near the object test—for the case of this study a non-magnetic plate—, and as a result of induction, eddy currents are generated. A secondary magnetic field is generated due to the eddy currents, and by measuring this secondary magnetic field from the receiver coil, vast information can be extracted and used to characterise surface and subsurface cracks, since the secondary field depends on the electromagnetic (EM) properties of the non-magnetic object.

Similar systems have been reported, for measuring the flow levels [6], the work presents a single operation frequency from 100kHz up to 10MHz, and [7] is one of the first in reporting the demodulation using only half of the period of the signal of interest. In addition, an induction instrument developed for a biomedicine application is reported in [8]. On the next section a description of the system is presented, divided in hardware, and software subsections.

3 System Design

The hardware is divided into three different components, the sensor (pair of coils), signal conditioning board, and the process/data acquisition board, where the FPGA is the main device. This device configuration is depicted in Figure 1.

The conditioning board consists mainly of an amplification stage; this is due to a relatively small signal response. The processing board is composed by: the interface for the data acquisition (DAQ), demodulation process, and serial USB communication. The processing board is depicted in Figure 2, and all of these different functions are performed by the FPGA.

The FPGA used is a Xilinx Spartan 3, XC3C400, which performs the interface with a high-speed rate A/D converter (10 MSPS, and 14 bits resolution) and with the D/A converter with a conversion rate of 165 MSPS and 14 bits resolution. The main issue in the DAQ module is the difference in time sample rate. To overcome this obstacle, the module is interfaced with a single clock rate of 10MHz. The serial USB communication is interfaced with the FPGA and
PC Host through CY7C68013A; the FPGA generates the interface signal in order to establish communication.

The FPGA, which is reprogrammable, is able to perform a high number of instructions that provide a viable solution to process a vast amount of information with a single element. This feature gives the advantage to employ the FPGA in signal generation and demodulation process. In the next subsection, the demodulation and signal generation are discussed.

3.1 Signal generation

The digital signal generation is carried out by using a Xilinx IP core, the Direct Digital Synthesizer (DDS). This IP core generates an arbitrary signal using a fix clock reference, applying the IP core provides the option to generate two different signals: sine and cosine waveforms, which can be converted to an analogue form with the D/A interface.

3.1.1 Single Frequency

The single frequency signal generated with the IP core has the following form:

\[ S(t) = A_s \cdot \cos(2\pi f_m t + \phi_s) \]  

where \( A_s \), \( f_m \), \( \phi_s \) is the amplitude, the frequency, and the phase of the excitation signal respectively. The generated signal is applied to the excitation coil through the D/A converter interface, having the form:

\[ V(t) = A_m \cdot \cos(2\pi f_m t + \phi_m) \]  

where \( A_m \) is the amplitude, \( f_m \) is the frequency, and \( \phi_m \) is the phase of \( V(t) \). This voltage is modulated, delayed by the interaction of the testing object. The signal response is captured by A/D, digitalizing the response voltage, the signal have the discrete form of (4)

\[ V[n] = A_m \cdot \cos\left(\frac{2\pi f_m n}{f_s} + \phi_m\right), \quad 0 \leq n \leq N_s - 1 \]  

where \( n \), \( f_s \), \( f_m \), \( \phi_m \) and \( N_s \) is number of sample in a cycle, the frequency, the sampling frequency, the frequency phase, and total number of samples respectively.
3.1.2 Multi-frequency

The multi-frequency signal generated has the form:

\[ S(t) = A_s \cdot \left( \cos(2\pi f_{m_1} t + \varphi_{s_1}) + \cos(2\pi f_{m_2} t + \varphi_{s_2}) + \cdots + \cos(2\pi f_{m_n} t + \varphi_{s_n}) \right) \]  

(5)

where \( A_s \) is the amplitude, \( f_{m_1}, f_{m_2}, \ldots, f_{m_n} \) are different frequency components of the signal, and \( \varphi_{s_1}, \varphi_{s_2}, \ldots, \varphi_{s_n} \) are the phases under different frequencies, this scheme of generation is depicted in Figure 3.

The multi-frequency signal captured by A/D converter has the form

\[ V[n] = A_m \left( \cos \left( \frac{2\pi f_{m_1} n}{f_s} + \varphi_{m_1} \right) + \cdots + \cos \left( \frac{2\pi f_{m_n} n}{f_s} + \varphi_{m_n} \right) \right), \quad 0 \leq n \leq N_s - 1 \]

(6)

where \( n \) is sample number in a cycle, \( f_{m_1}, \ldots, f_{m_n} \) number of component in multi-frequency mode, \( f_s \) is the sampling frequency, \( N_s \) is the total number of samples per cycle, and \( \varphi_1, \ldots, \varphi_{m_n} \) are the phase of each component.

![Figure 3 Multi-frequency signal implementation module](image)

3.2 IQ-Demodulation Process

3.2.1 Single Frequency Demodulation Process

The demodulation process is performed using a MACC (Multiplication and accumulation), an I/Q demodulation was used to reproduce the amplitude and phase of the response signal. The MACC module is used to multiply the digitized response signal (7) and reference signal (sine and cosine) generated by the DDS and stored in a look-up table inside the FPGA. The structure for the single demodulation process can be described with the equations

\[ I[n] = V[n] \times \cos \left( \frac{2\pi f_{m_1} n}{f_s} \right) = \frac{1}{2} A_m \cos(\varphi_m) + \frac{1}{2} A_m \cos \left( \frac{4\pi f_{m_1} n}{f_s} + \varphi_m \right) \]

(7)

\[ Q[n] = V[n] \times \sin \left( \frac{2\pi f_{m_1} n}{f_s} \right) = \frac{1}{2} A_m \sin(\varphi_m) + \frac{1}{2} A_m \sin \left( \frac{4\pi f_{m_1} n}{f_s} + \varphi_m \right) \]

(8)
$I[n]$ and $Q[n]$ are the in-phase and quadrature components respectively, $n$ is the number of sample in a cycle, $f_s$ as sampling frequency and $\varphi_m$ the frequency phase.

Once $I[n]$ and $Q[n]$ are obtained the signal pass through a low pass filter, and the real part and imaginary of the digitized signal are derived by

$$X[n] = I[n] \otimes F[n] \approx \frac{1}{2} A_m \cos(\varphi_m) \quad (9)$$

$$Y[n] = Q[n] \otimes F[n] \approx \frac{1}{2} A_m \sin(\varphi_m) \quad (10)$$

where $X[n]$ and $Y[n]$ are proportional to the real and imaginary inductance.

### 3.2.2 Multi-Frequency Demodulation Process

The previous subsection described the single frequency demodulation, for the purpose of this paper the process was extended to a multi-frequency process; the schematic of it is depicted in Figure 4.

![Demodulation scheme implemented](image)

For the process depicted in Figure 4 the implementation is describe by the equations:

$$
\begin{align*}
I_1[n] &= V[n] \times \left( \cos \left( \frac{2\pi f_{m_1} n}{f_s} \right) \right) \\
I_2[n] &= V[n] \times \left( \cos \left( \frac{2\pi f_{m_2} n}{f_s} \right) \right) \\
& \vdots \\
I_n[n] &= V[n] \times \left( \cos \left( \frac{2\pi f_{m_n} n}{f_s} \right) \right)
\end{align*}
$$

(11)
\[
\begin{align*}
Q_1[n] &= V[n] \times \left( \sin \left( \frac{2\pi f_{m_1} n}{f_s} \right) \right) \\
Q_2[n] &= V[n] \times \left( \sin \left( \frac{2\pi f_{m_2} n}{f_s} \right) \right) \\
&\vdots \\
Q_n[n] &= V[n] \times \left( \sin \left( \frac{2\pi f_{m_n} n}{f_s} \right) \right)
\end{align*}
\]

Once again \(I_1[n], I_2[n], \ldots, I_n[n]\) and \(Q_1[n], Q_2[n], \ldots, Q_n[n]\) represent the in-phase and quadrature components respectively, and the subscript in each variable represents the number of frequency demodulated, \(n\) is the number of sample in a cycle, \(f_s\) as sampling frequency and \(f_{m_1}, \ldots, f_{m_n}\) are the frequency component.

As in the single frequency demodulation process, \(I_1[n], I_2[n], \ldots, I_n[n]\) and \(Q_1[n], Q_2[n], \ldots, Q_n[n]\) are filtered by a low pass filter, represented by the equations (13) and (14)

\[
\begin{align*}
X_1[n] &= I_1[n] \otimes F[n] \approx \frac{1}{2} A_m \cos(\phi_{m_1}) \\
X_2[n] &= I_2[n] \otimes F[n] \approx \frac{1}{2} A_m \cos(\phi_{m_2}) \\
&\vdots \\
X_n[n] &= I_n[n] \otimes F[n] \approx \frac{1}{2} A_m \cos(\phi_{m_n})
\end{align*}
\]

\[
\begin{align*}
Y_1[n] &= Q_1[n] \otimes F[n] \approx \frac{1}{2} A_m \sin(\phi_{m_1}) \\
Y_2[n] &= Q_2[n] \otimes F[n] \approx \frac{1}{2} A_m \sin(\phi_{m_2}) \\
&\vdots \\
Y_n[n] &= Q_n[n] \otimes F[n] \approx \frac{1}{2} A_m \sin(\phi_{m_n})
\end{align*}
\]

The equations (13) and (14) represent the proportional value for the real and imaginary inductances of each frequency component defined with subscripts in each equation. It is important to note that the filter has a zero crossing points at \(k f_s / N_A\), where \(N_A\) is the averaging points, and \(k\) are the second harmonics from the equations (5-6)[7]. For the case of the compound signal, this demodulation works with the zero crossing point of the lowest frequency on the look up table. This is a simple but powerful demodulation process, due to the high speed compared with some existing methods [7].

### 3.3 Software

The GUI software resided in the PC host has the function of receiving commands from the PC through an USB link and, both proportional real and imaginary inductance is displayed in Figure 5.
4 Results

The scheme adopted for the multi-frequency signal evaluation was a closed-loop, the experiments were performed without connecting the probe. This experiment allows the evaluation of the FPGA generation module and can be calibrated before the sensor is connected. The experiments scheme is presented in Figure 6.

Several experiments were performed using a single frequency and multi-frequency signals. The multi-frequency experiments consist of signals with components of two, four, six, and seven-frequencies. The signal noise ratio (SNR) of the signal generated in the FPGA was measured; the experiment was repeated 10 times for each scheme mentioned, in order to evaluate the consistency in the generation of the signal.

For a single frequency, the experiment was conducted using frequencies from 10KHz-100KHz, the average SNR measured from these experiments was $\approx 84\, dB$, and the behaviour is depicted in Figure 7.
Several experiments for the multi-frequency evaluation were performed; Table 1 shows the experiments scheme. The first row mentions the component frequencies number, the second row is for different experiments configurations, and last row presents the configuration experiments. In the case of the single frequency presented in the first column, there were 10 different configurations of experiments due to step selected in the frequency, the initial configuration was selected at 10KHz, up to 100KHz with a step of 10KHz.

Table 1 Configurations Experiments

<table>
<thead>
<tr>
<th>Frequency Components</th>
<th>Experiments Configurations</th>
<th>Configurations</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>10</td>
<td>10KHz-100KHz</td>
</tr>
<tr>
<td>2</td>
<td>9</td>
<td>10KHz&amp;20KHz, 10KHz&amp;30KHz, 10KHz&amp;40KHz, 10KHz&amp;50KHz, 10KHz&amp;60KHz, 10KHz&amp;70KHz, 10KHz&amp;80KHz, 10KHz&amp;90KHz, 10KHz&amp;100KHz</td>
</tr>
</tbody>
</table>
| 4                    | 3                         | 1.- 10KHz, 20KHz, 30KHz, 40KHz  
                          |   2.- 10KHz, 50KHz, 60KHz, 70KHz  
                          |   3.- 10KHz, 80KHz, 90KHz, 100KHz |
| 6                    | 2                         | 1.- 10KHz, 20KHz, 30KHz, 40KHz, 50KHz, 60KHz 
                          |   2.- 10KHz, 60KHz, 70KHz, 80KHz, 90KHz, 100KHz |
| 7                    | 2                         | 1.- 10KHz, 20KHz, 30KHz, 40KHz, 50KHz, 60KHz, 70KHz 
                          |   2.- 10KHz, 50KHz, 60KHz, 70KHz, 80KHz, 90KHz, 100KHz |

Using these sets of experiments the SNR was calculated for each number of frequency component; the averaged value of calculated SNR is presented in Figure 8.

Figure 8 SNR measured on the different experiments schemes

The following experiments conducted consist of the scanning of an aluminium plate, presented in Figure 9, the plate presents two different cracks, pits and lines cracks, the pits are located at the middle and the lines are at the side of the plate.
The frequency selected for the test was 60 KHz, this frequency was selected SNR derived from the chart presented in Figure 7. The Figure 11 is the measured signal response from the aluminium plate, as mentioned before the scan frequency was 60 KHz, the signal does not present disturbance. Conversely, the Figure 11 presents the signal response of the pits, the chart presents four pits with forward and inverse scanning manners.

5 Conclusions

The experiments scheme mentioned in the last section present the SNR behaviour for a multi-frequency signal; the inclusion of more signal component to the final signal generation will produce a drop in signal noise ratio about 4db. This relation can be seen on Figure 8. In summary, the main function modules for a magnetic induction measurement system have been developed based on the FPGA board. Single frequency signals ranging from 1 Hz to 2 MHz have been generated; multi-frequency composite signals with up to seven frequencies
components have also been discussed. The number of frequency components can be extended to arbitrary numbers and this offers distinct advantages for the intended measuring systems over traditional single frequency systems. The digital to analogue conversion and the demodulation process are also demonstrated. Simultaneous multi-frequency demodulation has been carried out with a good trade-off.

References


