NONDESTRUCTIVE ANALYSIS OF SIGNAL INTERCONNECTION ON THERMALLY ENHANCED BALL GRID ARRAY

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Abstract

As the package's complexity and compactness grow, the challenge of nondestructive analysis becomes more difficult for the ultra-fine pitched interconnections and the heat spreader structures. To confront this analysis issue, the ultrafine-pitch wirebond interconnect with thermally enhanced heat spreader attached to the ball grid array (BGA) package are analyzed. Time-domain reflectometry (TDR) is being used increasingly to characterize the interconnection of thermal enhanced BGA (EBGA). We have proposed a TDR method for determining EBGA fault location base on between test waveform and open waveform by using open-end fixture (OEF). An OEF was employed to detect the rapid rise of edge signals from the package and to monitor them under the two parameters of time interval and reflection voltage. The TDR measurement results can determine both the failure location and type based on the above-mentioned parameters for an EBGA package. Then, a detailed failure analysis is performed by X-ray to confirm the experimental findings.

1. Introduction

The semiconductor devices tend to increase functionally and performance on the smaller overall feature sizes with demanding fine pitch and thermal carrying capability required at the packaging technology in order to increase the functionality and reliability. Wirebond interconnect in the range of 25-um pitch and almost double thermal efficiency will become an industry standard by the year 2010 for the 2005 ITRS roadmaps [1, 2]. Various packaging methods have been developed to satisfy these needs. Particularly, the EBGA packages have been used for these applications due to their improved thermal and electrical performances with relatively low cost and size [3]. An EBGA of wirebond interconnect is developed to incorporate higher number of device I/O pin counts, increase power, and provide additional ground paths for signal integrity purposes [1]. However, the trend to reduce interconnect size further while simultaneously increasing package functionality contradicts each other in areas such as the ability to maintain a reliable package design features in a manufacturing environment. Consequently, wiresweeping from fine-pitched wire utilization and mold process control variations cause an open and a short circuit for the bond-wire.

Traditionally, electrical package failure analysis with the equipment and software for X-ray image has advanced rapidly in recent years [3-8]. The EBGA with heatspreader is an excellent package solution of high power and hence it is a poor failure analysis with X-ray. X-ray image is a nondestructive reading graphic process for capturing two or three-dimensional information about the internal structure of an object [6]. However, the interconnection structure of EBGA package is more and more complex, especially when there are more than two copper layers in the substrate, adhered heat sink, or when the assembly has more density. The difficulty on nondestructive analysis in EBGA package of multi-layer substrates using X-ray method has been increased extremely. Some of these defective packages cannot be detected because the limitation of the X-ray inspections technique.

In recent years, TDR technique has been found to be a very successful technique when used in the assembly and packaging industry to evaluate the standard plastic packing technologies such as SOPs (Small outline package) Mf-BGA (Mounting frame BGA) [9] and BGA's [10-12], and FC-BGA [13]. TDR technique was initially developed for locating on long electrical systems such as telephone wires, network lines, and optics transmission paths [14, 15]. Thus, TDR is a powerful and novel measurement technique that uses for detecting the location of opens and shorts on signal lines on IC packages. These studies were aimed at the determination of the package failure analysis. This paper will demonstrate the effectiveness of TDR at non-destructively analyzing a range of advanced EBGA packaging technologies. TDR was used to analyze the location of open- or short-circuit defects in four main regions of EBGA packaging. The

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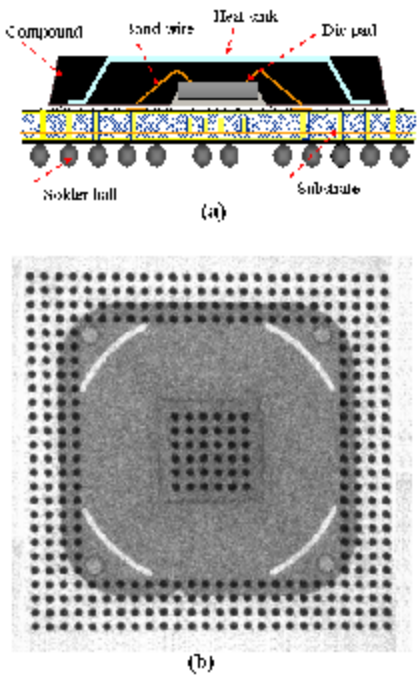


Figure 1: *(a) Cross section drawing of EBGA package and (b) top view X-ray picture.*

begins with the presentation of the proposed method. Subsequently, the fault analysis and verification is introduced. Finally, the experimental results and discussion are demonstrated.

2. Measurement setup

2.2. Test Example of EBGA

The test example for this experiment is a 35×35×1.5 mm body size of EBGA package for this study. The top and cross-sectional view of the test example is shown in Fig. 1. Fig. 1(a) shows cross section of EBGA that consists of heat-spreader, chip, molding compound, Bismaleimide Triazine (BT) Resin, bond wire and solder ball. The EBGA package construction consists of a copper heatspreader (or heat sink) placed over the chip and molded into the package, exposing only the top surface of the heatspreader. The EBGA with heatspreader is an excellent package solution of high power and hence it is a poor analysis of failure with standard X-ray is shown in Fig. 1(b). The EBGA package with a 388 solder ball count and 1.27 mm ball pitch is the failure device of the assembly vehicle for this study. The EBGA ball is 0.76 mm in diameter and is solder attached to the two-layer BT resin. The chip size is 10-mm × 10-mm and both dies have a single row of perimeter Al terminal pads.

The reason for this selection is that the package can calibrate a large die-to-package ratio impact on nondestructive analysis of the interconnection.

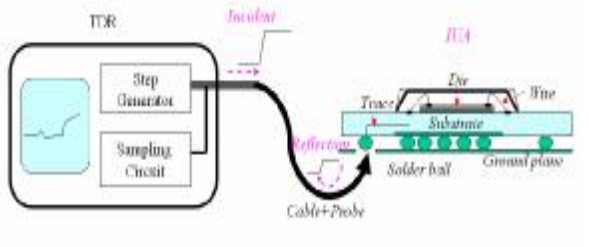


Figure 2: *Schematic drawing of the measurement setup*

Accordingly, the results found on the die-to-package area ratio can be extended further as an inference point to manufacture in the next generation of electrical packaging, which high-density without significantly increasing and improved thermal dissipation capability their dimensions.

2.2. Measuring System

The configuration of the TDR system is shown in Fig. 2. The analysis structure was constructed by OEF of homemade connected to an Agilent 86100A Infiniium DCA (Digital communications analysis) with A54754A dual-channel TDR module. The system includes a sampling oscilloscope, a step generator that with fast risetime, an OEF, a personal computer. All components are commercially available except the OEF. A computer is employed to process the data waveform from the TDR. This sampling head has a rectangular pulse with a fast transition between its baseline (nominally 0 V) and its topline (nominally 400 mV). The risetime of 50 ps was propagated through the OEF onto the package interconnection. The NA system is a digital oscilloscope with a very high sampling rate, which will record the magnitude and time interval of the reflected voltage signal simultaneously.

2.2. Test fixture description and design

General probe tip can not directly connect to solder ball of EBGA, and therefore must make an OEF for probing. The design of the OEF consists of four main parts: (1) open-end semi-rigid coaxial probe, (2) patterned pogo-pin array, (3) copper film, and (4) pogo pin house. This OEF combined pogo pin array with copper film as shown in Fig. 3. The coaxial line was filled with a lossless homogeneous dielectric with a relative dielectric constant ε_r=2.1. In order to isolate unequivocal the short between two interconnections and enhance the accuracy of failure location in EBGA packages, the other balls were shorted to ground.

2.2. System calibration

Multiple reflections can be it difficult the correct impedances and delays in a voltage curve. To calibrate a TDR approach involves the use of known standard impedances to calibrate the TDR system with SMA-connector calibration kit, which three chosen standards were the short, the open, and a reference 50 Ω. The calibration corrects for the error caused by the response of the measurement system. For a 35 ps TDR system of Agilent 86100A Infiniium DCA, such a bandwidth would be on 10 GHz.

In the analysis, the pulse generator lunched a square pulse with rising time less than 35 ps to the OEF. It is a voltage step pulse with a risetime of approximately 50 ps after its connect OEF. However, the reference planes can be depending on the SMA connector calibration. Therefore, for the OEF calibration is not required. For OEF calibration of TDR an extreme calibration required to adjust the delay of the open-standard signal. After adjusted delay time, the system recorded the reflected waveform and passed it to computer for further analysis. Averaging function of the TDR system was used remove the measurement noises as much as possible.

3. Theoretical background

3.2. Transmission line theory

A transmission lines to analyze the interconnection effects on the EBGA, the electrical characteristic of the interconnection must be defined. The basic electrical characteristics define a transmission line are the characteristic impedance and propagation velocity. Transmission line refers to any pair of conductors that can transmit an electrical signal from one end to the other. They include parallel-plate, two-wire and coaxial lines. A transmission line is a distributed parameter network and is described by circuit parameters that are distributed throughout its length [16]. It has been shown in [16] that in the transmission line model a two-conductor can be characterized by its parameters R (resistance per unit length), L (inductance per unit length), G (conductance per unit length), and C (capacitance per unit length). For the characteristic impedance and the propagation velocity of interconnection lines are determined by:

$$Z_{line} = \sqrt{\frac{(R + jwL)}{(G + jwC)}} \tag{1}$$

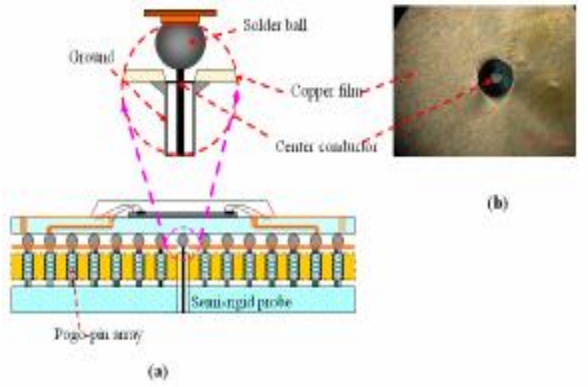


Figure 3: *(a) Cross section drawing of the OEF Configuration and (b) top view.*

$$v_p = \frac{c}{\sqrt{e_r}} \tag{2}$$

where ε_r is the relative dielectric constant of the media and c is the speed of light in vacuum(3×10^8 m/sec). In TDR, the signal gets reflected at each plane and some of it may travel back to the source. The theory goes that, the voltage reflection coefficient (ρ), which is defined as the ratio of the reflected voltage ($V_{reflected}$) to the incident voltage ($V_{incident}$), is simply determined by the conductor impedance Z_i at the reflection plane, and is related to the multi-section of conductor impedance by the equation [17]:

$$r_{i=} = \frac{V_{reflected}}{V_{incident}} = \frac{Z_i - Z_{i-1}}{Z_i + Z_{i-1}} \tag{3}$$

where Z_i is the characteristic impedance of the *i*-th section, Z_{i-1} is the characteristic impedance of the *i-1*-th section, and *i* is the direction of propagation from the incident waveform.

The characteristic impedance Z_{TL} of the transmission line can be written in terms of the voltage reflection coefficient [18]:

$$Z_{TL} = \frac{1+r}{1-r} Z_0 \tag{4}$$

where Z_0 is the electrical impedance of the TDR head and is typically about 50 Ω. The measured reflected voltage is a sum of $V_{incident}$ and $V_{reflected}$, so that $V_{reflected} = V_{measured} + V_{incident}$. Substitute the equation $V_{reflected} = V_{measured} + V_{incident}$ into equation (3) and equation (4) gives:

$$V_{measured} = \frac{2Z_{TL}}{Z_{TL} + Z_0} V_{incident} \tag{5}$$

In TDR, a fast-rise step voltage electromagnetic pulse is propagated in the medium of EBGA along

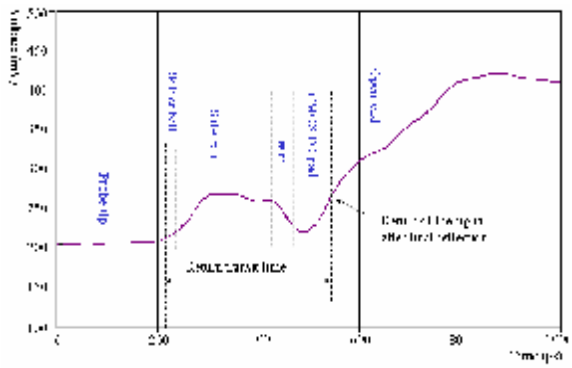


Figure 4: *Measured waveform of solder ball, substrate trace, bonding wire, and CMOS I/O pad.*

an interconnection line. The TDR records a waveform edge expressed by the voltage or reflection coefficient as function of time [19]. The transit time (t) of the TDR pulse propagating one return trip along an interconnection line of length (L_m) is represented by:

$$L_m = \frac{ct}{2\sqrt{e_r}} \tag{6}$$

3.2. Failure location and type

TDR sends a fast rising edge of step voltage down the signal and ground wire, which reflects at any impedance discontinuity such as an open or short circuit in the metal wire. The magnitude and polarity of the reflected signal tells the type of fault, and the delay time between the incident and reflected signals tells the distance to the fault interconnection. The fault type is based on the comparison of the fault-free voltage (V_{ff}), measured voltage (V_{iut}) at the interconnection under test, defined by the error function:

$$V_{ef}(t) = V_{ff}(t) - V_{iut}(t) \tag{7}$$

The fault types are detected as follows:

$$F_{ef} = \begin{cases} Max(V_{ef}(t)) > V_t, & open\_fault \\ Min(V_{ef}(t)) < -V_t, & short\_fault \\ others \quad , & fault\_free \end{cases} \tag{8}$$

where V_t is the threshold voltage, $Max(\cdot)$ is the largest of the voltage difference between fault-free and measure voltage, and $Min(\bullet)$ is the smallest of the voltage difference between fault-free and measure voltage. The threshold voltage may be used to quantify the tolerance range. If the voltage of $V_{ef}(t)$ is not within the tolerance range the interconnection is declared faulty.

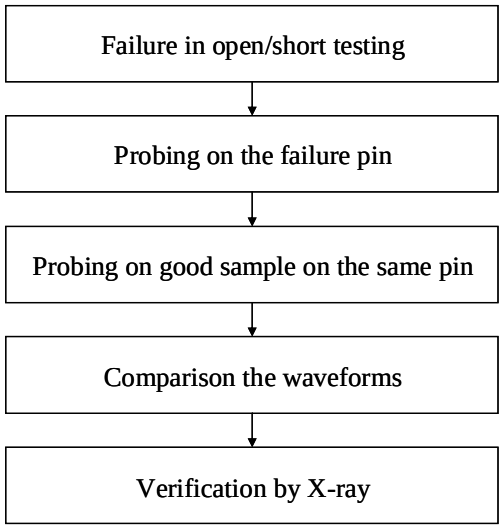


Figure 5: *Open and short circuits detection procedure.*

The fault location from the monitoring point at the scope to the point of fault is given by [11]:

$$L_f = \sum_{i=1}^{n} \frac{c \times T_p}{2\sqrt{e_{r,i}}} \tag{9}$$

where n is the section of package, T_p is the time interval from monitoring point to the fault back again, and ε_{rj} is the effective dielectric constant of the ith segment. Fig. 4 shows a typical capture of a TDR response for the EBGA package. This time (T_p) can easily be determined from the trace of the reflected signal recorded by the TDR.

4. Nondestructive analysis and verification

To verify the TDR technique of nondestructive analysis, a comparative analysis of x-ray finds the TDR waveform in EBGA interconnection for the open and short-circuits failure. These fault types and location analysis included: open at the solder ball, open at the substrate, short between two solder balls, short between two bond wires, and short to I/O pad. In order to identify the open or short location in the EBGA packages, a comparative TDR measurement was applied to compare the known good waveform with the waveform that measured. By analyzing the position and voltage of the echoes, a number of characteristics about the interconnection can be determined including the distance to opens or shorts circuit. Fig. 5 shows the detecting process for open and short circuit defect by the TDR approach and X-ray.

4.2. Open circuit fault

Interconnection containing defects that lead to a complete break of an interconnection is called an

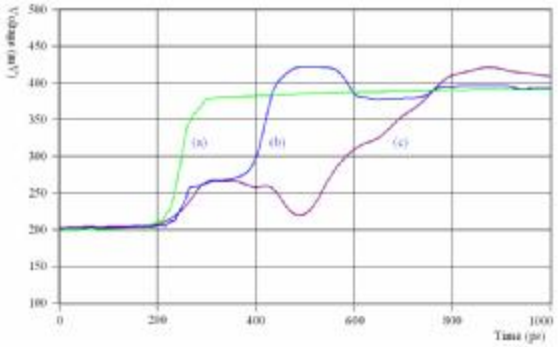
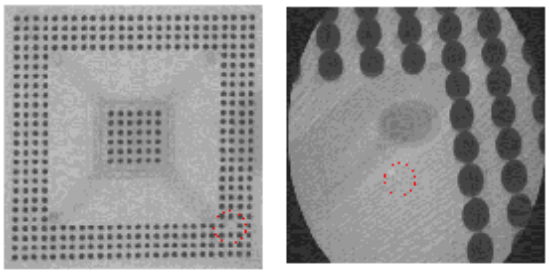


Figure 6: *Waveforms of open failure curve. (a) Open in the solder ball and (b) open failure curve of substrate.*



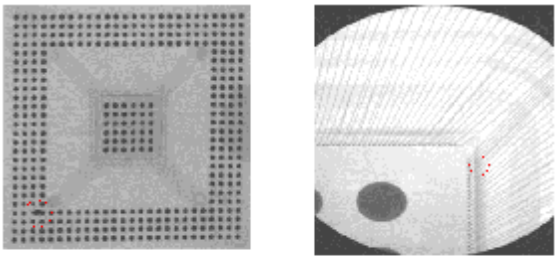
(a) (b)

Figure 7: *Top-down X-ray micrograph of a failing site for removed-heatspreader. (a) Open in the solder ball and (b) broken copper interconnection traces after the package molding. Circles mark the failure points.*

open fault. TDR measurement on defect-free interconnection and three signal traces with an open defect are shown in Fig. 6. The incident voltage of Fig. 6 (a) & (b) are approximately 200 mV in amplitude and the reflected voltage bumps the voltage up to 400 mV at t = 220 ps and 380 ps, which aggress with the top-down X-ray inspection in Fig. 7(a) & (b). The X-ray micrograph of a failing site, (a) open in the solder ball, and (b) broken copper interconnection traces after the package molding. Circles identifications from design mark the failure points.

4.2. Short circuit fault

Interconnection containing defects leading to a bridge of two individuals of interconnection or a connection to ground/power plane are called a short fault. Fig. 8 shows top-down X-ray micrograph of a failing site after removal heatspreader. Fig. 8 (a) Short in the solder ball, and (b) the bridged Au wire in the chip side. Circles identifications from design mark the failure points. Fig. 9 indicates a short fault on the EBGA because the TDR waveform has negative polarity. The voltage decreases down occur at 280 ps and 370 ps,



(a) (b)

Figure 8: *Top-down X-ray micrograph of a failing site for removed-heatspreader. (a) Shorted solder ball and (b) the bridged wire in the bond wire region. Circles mark the failure sides.*

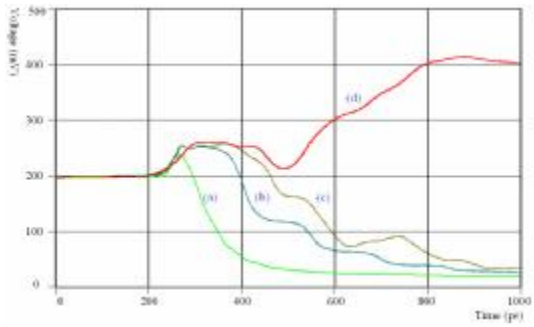


Figure 9: *Waveforms for short failure curve. (a) Shorts between two solder balls, (b) short failure curve of bridged wire, and (c) short failure curve of I/O pad of chip.*

which correspond with Fig. 8 (a) & (b). Fig. 8 (c) indicates a short fault on the I/O pad, but it is a failure analysis with X-ray image.

5. Experiential results and discussion

For the samples with open failure and short failure, the images obtained by X-ray are shown in Figs. 7 and 8. As shown in the experimental results, X-ray images have confirmed the analytical findings for TDR analysis method. TDR waveform displays the locations of manufacturing faults on the location of the EBGA interconnection, to identify opens or shorts. The most challenging aspect of comparative TDR analysis includes distinguishing either a failure in the bonding finger of the substrate or in the die pad, because the TDR measurement in these two regions had similar waveforms. To help failure analysis in this area, we can build the database of well-known waveforms associated with each failure site for a specific type of interconnection impedance. Thus, TDR analysis can be a nondestructive method to determine the exact failure location of BGA assemblies.

In Fig. 4 shows the good package of curve-ends with a relatively large capacitive, so the resulting in the "V" trailing ends of the TDR waveform for I/O pad of CMOS. By comparing with the reference waveform, the package-containing defect can be easily distinguished. It should be noted that, since the TDR is reflected at the end of open/short and does not be used to detect the second fault in the same interconnection. The fault of the same interconnection can only be measured by the first fault of closing OEF tip for an open or a short circuit. In other words, the same trace of the interconnection cannot be used to detect short-circuit and open-circuit fault at the same time. But it can be used to measure impedance mismatches when there are more than one physical fault. The TDR nondestructive analysis is unable to distinguish shape and size of defects, but it can detect the locations of defect.

The spatial resolution of the TDR defines the precision of localization of the failures by the risetime of the incident signal, the quality of the measurement cable and connectors, and the bandwidth of the digital oscilloscope. The overall system risetime can be expressed as a function of the individual risetimes using the following relation:

$$t_{total} = \sqrt{t^2_{incident} + t^2_{scope} + t^2_{cable} + t^2_{connector} + t^2_{OEF}} \qquad (10)$$

where $t_{incident}$ is the risetime of incident signal, t_{scope} is the risetime of oscilloscope, t_{cable} is the risetime of cable, $t_{connector}$ is the risetime of connector, t_{OEF} is the risetime of OEF. Indeed, two adjacent discontinuities in a transmission line will be distinguishable by the measurement system only if their distance is higher than the spatial resolution. The spatial resolution in a interconnection is defined as [20]:

$$\mathbf{l}_{resolution} = \frac{ct_{total}}{2\sqrt{e_{eff}}} \qquad (11)$$

From equations (10) and (11), the bandwidth of the overall system is the main limiting factor and a poor characteristic element in the measurement system will affect its performance.

6. Conclusions

In this paper, we develop and demonstrate a nondestructive evaluation technique using TDR for the EBGA interconnection. An OEF was employed to detect the rapid rise of edge signals from the package and to monitor them under the two parameters of time interval and reflection voltage. The TDR measurement results can determine both the failure location and type based on the above-mentioned parameters for an EBGA package. To double-check the data consistency, these faults analysis are performed by X-ray to confirm the experimental findings.

7. Acknowledgements

This work was supported by the National Science Council, Taiwan, R.O.C. under contract No. NSC 95-2221-E-006-016. Also, this work made use of Shared Facilities supported by the Program of Top 100 Universities Advancement, Ministry of Education, Taiwan.

8. References

[1] Chung, S. and Shi, F. G., "Process and Design Analysis for Ultrafine-Pitched Wiresweep Elimination in Advanced Copper Heat Spreader BGA Package," IEEE Trans. Advanced Packaging, 28(2):278-287, 2005.

[2] "International Technology Roadmap for Semiconductors 2005 Edition- Assembly and Packaging," Semiconductor Industry Association, URL:http://www.itrs.net/Common/2005ITRS/.

[3] Marrs, R. C., et al., Ball Grid Array Technology, McGraw-Hill Book Company Inc., USA, 1995.

[4] Moore, T. D., Vanderstraeten, D., and Forsell, P., "Determination of BGA Structural Defects and Solder Joint Defects by 3D x-ray Laminography," in *IEEE Proc. of 8th IPFA*, 146-150, 2001.

[5] Ohring, M., "Reliability and Failure of Electronic Material and Device", Academic Press, San Diego, 1998.

[6] Thomas, D. M., and John, L. J., "Failure Analysis and Stress Simulation in Small Multichip BGAs," *IEEE Trans. Adv. Packag.*, 24(2):216-223, 2001.

[7] Bord, S., Clement, A., Lecomte, J. C., and Marmeggi, J. C., "An X-ray tomography facility for I.C. industry at STMicroelectronics Grenoble," *J. Microelectronic Eng.*, 61-62:1069-1075, 2002.

[8] Moore, T. D., Vanderstraeten, D., and Forssell, P.M., "Three-dimensional x-ray laminography as a tool for detection and characterization of BGA package defects," *IEEE Trans. Comp. Packag. Tech.*., 25(2):224-229, 2002.

[9] Ang, S., Meyer, D., Thach, T., Schaper, L., and Brown, W.D., "The Mini Flex Ball-Grid-Array Chip-Scale Package," IEEE/CMPT Electronic Packaging Technology Conference, 13-17, 1998.

[10] "Electronic Package Failure Analysis Using TDR", TDR System Application Note, URL: http://www.tdasystems.com.

[11] Chen, M. K., Tai, C. C. and Huang, Y. J., "Nondestructive Analysis of Interconnection in Two-die BGA Using TDR", IEEE TRANS. ON INSTRUMENTATION AND MEASUREMENT, 55(2):400-405, 2006.

[12] Abessolo-Bidzo, D., Poirier, P., Descamps, P., and DomengÃÃs, B., "Isolating failing sites in IC packages using time domain reflectometry: Case studies," Microelectronics Reliability Volume: 45(9-11): 1639-1644, 2005.

[13] Lihong, C., Chong, H. B., Chin, J. M., and Master, R. N., “Non-destructive analysis on flip chip package with TDR and SQUID,” in Conf. Electron. Packa. Tech., 50-55, 2002.
[14] Somlo, P. I., and Hollway, D. L.: “Microwave locating reflectometer,” Electron. Lett., 5:468-469, 1569.
[15] Philen, L., White, I. A., Kuhl, J. F., and Mettler, S. C., “Single-mode fiber OTDR: Experiment and theory,” IEEE Trans. Microw. Theory and Tech., 82(10):1487-1496, 1982.
[16] Stanghan, C. J. and Macdonald, B. M., “Electrical Characterization of Packages for High-speed Integrated Circuits,” IEEE Trans. Compon. Hybrids and Manuf. Technol., 8(4):468-473, 1985.
[17] Hayden, L. A. and Tripathi, V. K., “Characterization and modeling of multiple line interconnections from TDR measurements,” IEEE Trans. Microw. Theory and Tech., 42(1):1737-1743, 1994.
[18] Paulter, N. G., “An Assessment on the Accuracy of Time-Domain Reflectometry for Measuring the Characteristic Impedance of Transmission Lines,” IEEE Trans. Instrum. Meas Tech., 50(5):1381-1388, 2001.
[19] “Time Domain Reflectometry Theory,” Hewlett Packard Application Note 1304-2, 1988.
[20] Martens, L., High-frequency Characterization of Electric Packaging, Kluwer Academic, 1998.