Modular ultrasound arrays with co-integrated electronics

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Background/Motivation
Motivation: 2D Arrays

2D arrays can be used to produce volumetric, 3D images
   Fetal imaging, echocardiography

Large number of small individual elements (1,000-10,000) used
   Routing bottleneck due to fine pitch (λ pitch at 5MHz is 300 μm)
   Cable size prohibitive (~512 coax max)
   System channel limitation (256 system ch. vs. 2500 2D array ch.)
   Small 2D elements have significant attenuation due to cable loading

http://www3.gehealthcare.com/
Sparse arrays to reduce channel count (Holm, 1995)

Local electronics integrated at the probe

Sub Array Processors (SAPs) for local beamforming (Savord, 2003)

Switching matrix (Reconfigurable Arrays) to group elements (Erikson, 1996)

Improved sensitivity for small elements

Reduced channel count (256 channels instead of 2500, or 10000 channels)
Modular 2D Arrays
Large Area array: 100 x 100 elements, from 3cm x 3cm up to 20 cm x 20 cm
Transducer arrays integrated directly with Application Specific ICs (ASICs)
Area coverage achieved by tiling multiple acoustic/ASIC modules with organic interposer
“cMUTs” used as transducer technology

Potential advantages
  - Improved sensitivity for small elements (reduced loading, reduced crosstalk)
  - Reduced interconnect complexity (10,000 chs → 256 chs)

Challenges
  - Very dense electronics needed (unit cell must match transducer array pitch)
  - High voltage CMOS required (100Vpp transmit voltage)
Trenched capacitive Micromachined Ultrasound Transducer (MEMs fabrication)
Can be assembled using standard electronic packaging processes (flip-chip)
Electrical impedance higher than PZT (sensitivity issue)
Elements can have wide bandwidth (>90%)
“Trench/Frame” cMUTs used due to “Bulk” processing (equivalent to TSV)
Flip-Chip

Direct integration is ideal but very challenging (Daft et al, 2004)
Yield issues, Fab compliance, captive fab needed

Flip-chip integration is a good highly integrated alternative (Wygant et al, 2008)
Large array requires way to escape ASIC I/Os (e.g. TSVs)

Interposer (flex, ceramic, organic build-up) also used (Wodnicki et al, 2014)
Constraints: ASIC size, CTE mismatch, routing
Large Area 2D Array Prototype Implementation
Interposers used to create assembly mockup for tileable module
Interposer allows seamless tiling by covering gaps due to ASIC I/O pads
Prototype module dimensions: 2.4 cm x 4 cm, with 8x14 tiled array of cMUT chips
Total transducer channel count: 28,672
Double-sided flip assembly was used
Smaller and modular chips have higher yield and can select Known Good Die
Modular assembly was used with standard electronic packaging processes. Micro-BGAs (70 μm, Eutectic SnPb) attached to cMUTs by solder-jet process (PacTech). Pitch for assembly: 185 μm for cMUT devices, 150 μm for dummy ASICs. Under Bump Metallization (UBM) optimized to achieve uniformity of solder volume. Final thicknesses were: Ti/Ni/Au (0.015 μm/0.3 μm/0.1 μm). Substrate was dual-sided organic laminate build-up (Endicott Interconnect). Substrate routing: 9 layers, ~25um lines/spaces. Co-planarity: +/-10 μm (λ/10) local, 150 μm global (due to CTE mismatch).
Unit cell needs to match the size of the individual 2D transducer element
Low voltage switches 10-20x smaller than HV switches (local pulser used)
0.8 μm 2 metal, 50V CMOS/DMOS process
Lower $R_{on}$ better to mitigate signal attenuation
Results
Simulations were performed using Field II (Jensen, Med. Bio, 1996)
Annular array with 18mm aperture, 20 equal width rings
Element pitch was 185 μm for $f_c = 8$MHz and the focus was set at 50mm
Observed beamwidth: 0.69mm (both in elevation and azimuth)
Average side lobe energy: -40dB (for one-way simulation with 300 μm gaps)
Side lobes came up slightly (-35dB) with 93% element coverage (due to yield)
1.25D linear array, 3 x 192 ch. (32 x 192 cMUTs)
Dimensions: 6mm x 36mm
cMUT chip array (2 x 12) tiled on front surface
Dummy ASIC chips on backside (acoustic load)
Sensitivity decreased by shorted cMUT elements
  Low $V_{bias}$ and less active elements
Spatial resolution comparable to production GE PZT probe
Contrast resolution limited by poor sensitivity
Conclusions

Volumetric imaging requires large channel count 2D arrays

- Results in routing bottleneck and loss of sensitivity

Closely integrated cMUTs and ASICs were used to reduce channel count

Interposer-based modular, tiled architecture was used to improve yield

Acoustic simulations predicted acceptable image performance with gaps between transducer chips and missing elements

However, shorting of cMUT devices caused significant element loss resulting in reduced acoustic sensitivity and poor contrast resolution

Future work should address cMUT shorting directly in order to improve yield
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